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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,190	11/26/2003	Peter P. Altice JR.	M4065.0852/P852	6553

45374 7590 07/02/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

EXAMINER	
BEMBEN, RICHARD M	
ART UNIT	PAPER NUMBER
2622	
MAIL DATE	DELIVERY MODE
07/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,190	ALTICE ET AL.	
	Examiner	Art Unit	
	RICHARD M. BEMBEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *1,2,5,7-18,30-41 and 44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,19-21,23-29,42,43,45,46 and 48* is/are rejected.

7)☒ Claim(s) *22 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1, 2, 5, 7-18, 30-41 and 44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention or species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 31 March 2008.

Response to Arguments

2. Applicant's arguments filed 31 March 2008 have been fully considered but they are not persuasive.

3. Applicant traverses the 35 USC 103(a) rejection of claim 19 as being unpatentable over Kim in view of Beiley arguing that Kim teaches away from the combination because "Kim teaches that it is desirable to have as few elements as possible in the image sensor". Examiner disagrees. Kim does not teach that it is desirable to have as few elements as possible in the image sensor. Rather, Kim is directed toward sharing certain pixel circuitry among plural photodiodes (which ultimately reduces the number of transistors in an image sensor) and therefore does not teach away from a combination with Beiley.

Applicant supports his/her argument by citing Kim, Col. 2, lines 64-66 which broadly states that it is "an object of the present invention to provide a CMOS image sensor that may reduce its chip area by decreasing the number of transistor[s] for a pixel array [...]". However, it would be a misrepresentation of Kim's disclosed invention

to say that Col. 2, lines 64-44 is intended to mean that "it is desirable to have as few elements as possible in the image sensor". Kim teaches reducing chip area while maintaining similar functionality of prior art CMOS sensors by requiring plural photodiodes (Figure 4, "401" & "402") to share ("shared structure") a reset transistor ("M1"), a drive transistor ("M3") and a select transistor ("M4"); compare the prior art in Figure 2 with Figure 4. In summarizing the invention (Col. 7, lines 9-13), Kim states: "Since the photodiodes of the unit pixel according to the present invention share the reset transistor M1, the drive transistor M3 and the select transistor M4, the unit pixel according to the present invention may reduce its chip area as compared with the unit pixel according to the prior art."

Therefore, Kim is directed toward sharing a reset transistor, a drive transistor and a select transistor between two or more photodiodes (refer to Col. 7, lines 6-8), which ultimately does reduce chip area by decreasing the number of transistors. Since, the purpose of Kim's invention is sharing certain pixel circuitry among plural photodiodes and *not* that it is desirable to have as few elements as possible in the image sensor, Kim does not teach away from the combination with Beiley.

Regarding the rejection of claim 19 in non-final Office Action dated 31 December 2007, the examiner relied on Kim to disclose that plural photodiodes can share a reset transistor, a drive transistor and a select transistor in a CMOS image sensor. Beiley was relied on to teach an electronic shutter can be achieved in a CMOS image sensor by using a shutter transistor and a storage node. Since Kim does not teach away from a combination, a person having ordinary skill in the art of CMOS image sensors would

realize that an electronic shutter could be achieved in the image sensor disclosed by Kim via a shutter transistor and a storage node for each photodiode as disclosed by Beiley. Therefore, supplementing the teachings of Kim with Beiley achieve the required limitations of claim 19. As stated in non-final Office Action dated 31 December 2007, one would have motivation to do so in order to avoid using a mechanical shutter.

4. Regarding independent claim 3, 27 and 42, the same reasoning used in the discussion of claim 19, *supra*, for combining Kim and Beiley applies.

5. Regarding the dependent claims, the same reasoning used in the discussion of claim 19, *supra*, for combining Kim and Beiley applies.

6. Applicant's amendment to claim 28 overcomes the 35 USC 112, second paragraph rejection issued in non-final Office Action dated 31 December 2007. Therefore, this rejection is withdrawn.

7. For the reasons given, the art rejections given in non-final Office Action dated 31 December 2007 are repeated below (with the exception of claim 28, which is slightly modified).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 6, 19, 20 and 23-29, 42, 43, 46, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,731,335 issued to Kim et al., hereinafter "Kim" in view of U.S. 6,522,357 issued to Beiley et al., hereinafter "Beiley".

Claims 3 and 6 are method claims corresponding to apparatus claims 19 and 20. Therefore, claims 3 and 6 are analyzed and rejected as discussed below with respect to claims 19 and 20.

Regarding **claim 19**, Kim discloses a pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402");

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node (c. 4, l. 65 - c. 5, l. 15; Figure 4, "M43", "M44");

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said transfer gates (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" which is the source/drain diffusion of "M1"); and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M1", "M4").

However, Kim does not disclose a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor and a plurality of storage nodes, each node coupled to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors.

Beiley discloses a well-known CMOS image sensor pixel having an electronic shutter. The pixel comprises a photosensor (Figure 1, "14"), a shutter transistor (Figure 1, "pass transistor M2") connected to and transferring charge from a photosensor to a storage node (Figure 1, "node 2"), the node coupled to a respective shutter transistor and storing charge transferred by the photosensor (Figure 1, charge is stored at "node 2" via "capacitor 34"). Also refer to c. 3, ll. 20-35. Electronic shutters are implemented in digital cameras in order to avoid the additional expense, camera size, and complications that arise out of using a mechanical shutter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include shutter transistors and storage for each photosensor as disclosed by Beiley in the pixel circuit having plural photosensors disclosed by Kim. One would have motivation to do so in order to avoid using a mechanical shutter.

*Also refer to the discussion in **Response to Arguments.***

Regarding **claim 20**, refer to the rejection of claim 19 and Kim further discloses that said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer gates (c. 5, ll. 16-24; Figure 4, "M1").

Regarding **claim 23**, refer to the rejection of claim 19 and Beiley further discloses that said shutter transistor operates as an electronic shutter for said pixels (c. 1, ll. 10-13; c. 3, ll. 20-35).

Regarding **claim 24**, refer to the rejection of claim 19 and Beiley further discloses that said shutter transistor remains on during the integration period (c. 4, ll. 40-61, specifically ll. 49-51).

Regarding **claim 25**, refer to the rejection of claim 19 and Kim further discloses that said pixel is a CMOS pixel (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

Regarding **claim 26**, the combination of Kim with Beiley discloses a pixel that has five transistors (Kim: Figure 4, "M43, M44, M3"; Beiley: Figure 1, two "M2s").

Regarding **claim 27**, Kim discloses a pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402");

a transfer gate connected to said storage capacitor to transfer charge from said storage capacitor (c. 4, l. 65 - c. 5, l. 15; Figure 4, "M43", "M44");

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" which is the source/drain diffusion of "M1");

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M1");

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node (c. 5, ll. 16-24; Figure 4, "M3"); and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor (c. 5, ll. 16-24; Figure 4, "M4").

However, Kim does not disclose a shutter transistor connected to said photosensor to transfer charge from said photosensor and a storage capacitor connected to said shutter transistor to receive said charge transferred by said shutter transistor.

Beiley discloses a well-known CMOS image sensor pixel having an electronic shutter. The pixel comprises a photosensor (Figure 1, "14"), a shutter transistor (Figure 1, "pass transistor M2") connected to and transferring charge from a photosensor to a storage node (Figure 1, "node 2"), the node coupled to a respective shutter transistor and storing charge transferred by the photosensor (Figure 1, charge is stored at "node 2" via "capacitor 34"). Also refer to c. 3, ll. 20-35. Electronic shutters are implemented in digital cameras in order to avoid the additional expense, camera size, and complications that arise out of using a mechanical shutter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include shutter transistors and storage for each photosensor as disclosed by Beiley in the pixel circuit having plural photosensors disclosed by Kim. One would have motivation to do so in order to avoid using a mechanical shutter.

Also refer to the discussion in ***Response to Arguments.***

Regarding **claim 28**, refer to the rejection of claim 27 and Kim further discloses that a plurality of photodiodes and transfer gates share a floating diffusion node, reset transistor, source follower transistor, and row select transistor (c. 4, l. 65 - c. 5, l. 15; Figure 4, "node A" is shared by "401", "M43" and "402", "M44"). Based on the combined teachings of Kim and Beiley, it would have been obvious to a person having ordinary

skill in the art at the time of the invention that the shutter transistors storage capacitors disclosed by Beiley also share a floating diffusion node, reset transistor, source follower transistor, and row select transistor.

Regarding **claim 29**, refer to the rejection of claim 27 and Kim further discloses that said pixel is a CMOS pixel (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

Regarding **claim 42**, refer to the rejection of claim 19 over Kim in view of Beiley and Kim further discloses an imaging system comprising a processor (c. 1, ll. 25-60; Figure 1, A/D converter, comparator, CDS, control and interface can all be considered "processors"). *Also refer to the discussion in* ***Response to Arguments.***

Regarding **claim 43**, refer to the rejection of claim 42 and Kim further discloses that a number of said plurality of photosensors is two photosensors (c. 4, l. 65 - c. 5, l. 15; Figure 4, "401", "402").

Regarding **claim 45**, refer to the rejection of claim 42 and Beiley further discloses that said shutter transistor is an electronic shutter (c. 1, ll. 10-13; c. 3, ll. 20-35).

Regarding **claim 46**, refer to the rejection of claim 42 and Beiley further discloses that said shutter transistor remains on during the integration period (c. 4, ll. 40-61, specifically ll. 49-51).

Regarding **claim 48**, refer to the rejection of claim 42 and Kim further discloses that said imaging system is a CMOS imaging system (c. 2, ll. 64-67; c. 3, ll. 1-21; Figure 4).

10. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Beiley in further view of U.S. Patent No. 6,697,114 issued to Merrill.

Claim 4 is a method claim corresponding to apparatus claim 19. Therefore, claim 4 is analyzed and rejected as discussed below with respect to claim 19.

Regarding **claim 21**, Kim in view of Beiley disclose the limitations of claim 19, specifically storage nodes coupled to shutter transistors for storing charge transferred by photosensors. Beiley further discloses that the storage nodes are capacitors (Figure 1, "34"). While it is well-known that in integrated circuits capacitors are formed using layers of metallization above the substrate in which diffused layers exist, Kim in view of Beiley do not explicitly disclose that the capacitors are formed above the substrate in which the floating diffusion node is formed (diffused within).

Merrill discloses an image sensor pixel having plural photosensors and a shared readout structure where storage capacitors are formed above the substrate in which the floating diffusion node is formed (c. 5, ll. 9-24; "inherent gate capacitances" gate is metallization above the substrate). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form capacitors above the substrate as disclosed by Merrill in the storage nodes disclosed by Kim in view of Beiley, since that is typically how capacitors are created in integrated circuits.

Allowable Subject Matter

11. Claims 22 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art does not disclose the use of polypropylene capacitors for use in an electronic shutter circuit of an active pixel sensor.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD M. BEMBEN whose telephone number is (571)272-7634. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David L. Ometz/
Supervisory Patent Examiner, Art Unit 2622

RMB